


GA-78LMT-S2P

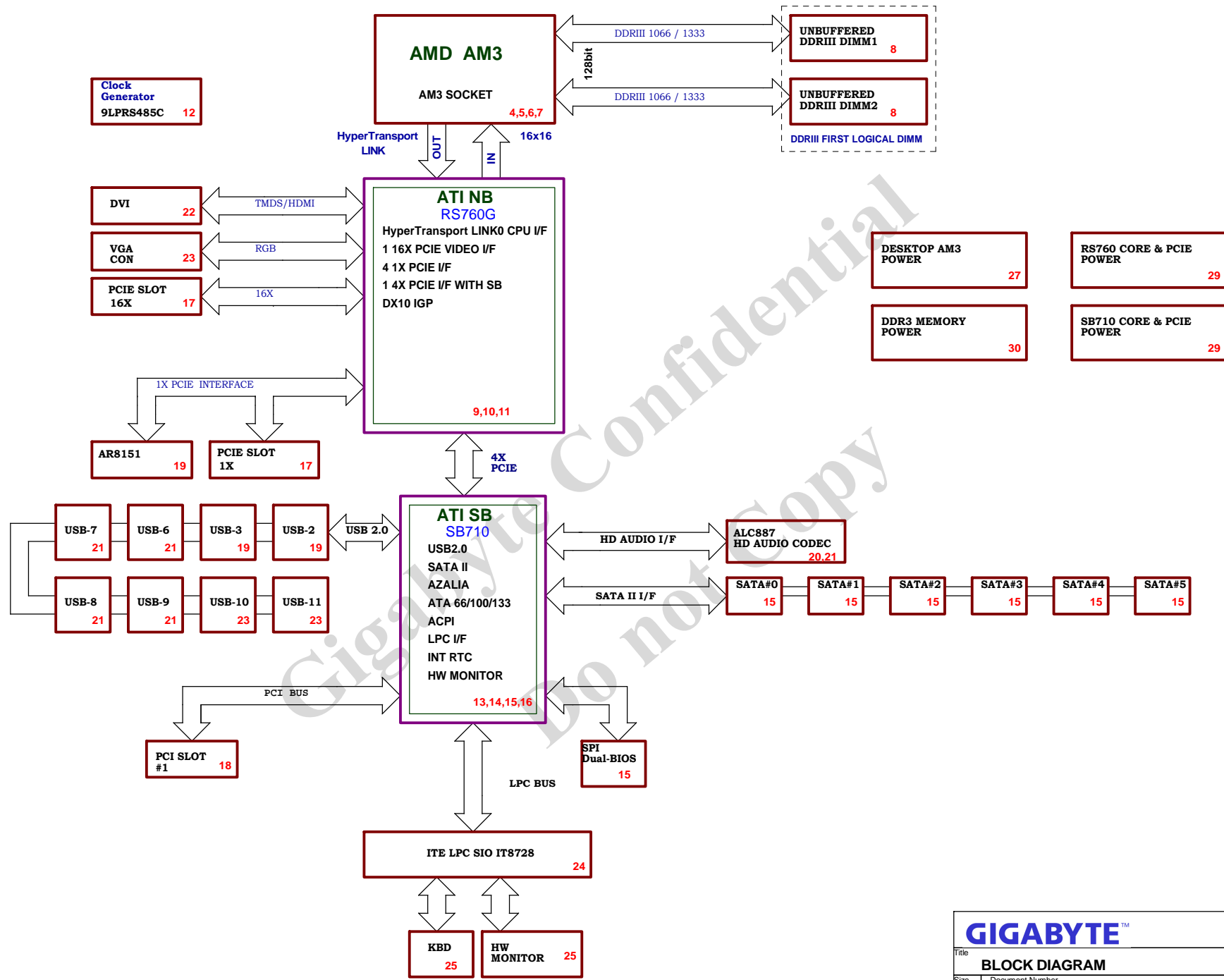
Revision : 5.02

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23	ATX, FRONT PANEL	
24	VCORE(RT8868+RT9612)	
25	POWER SEQUENCE,EUP	

[illegible]

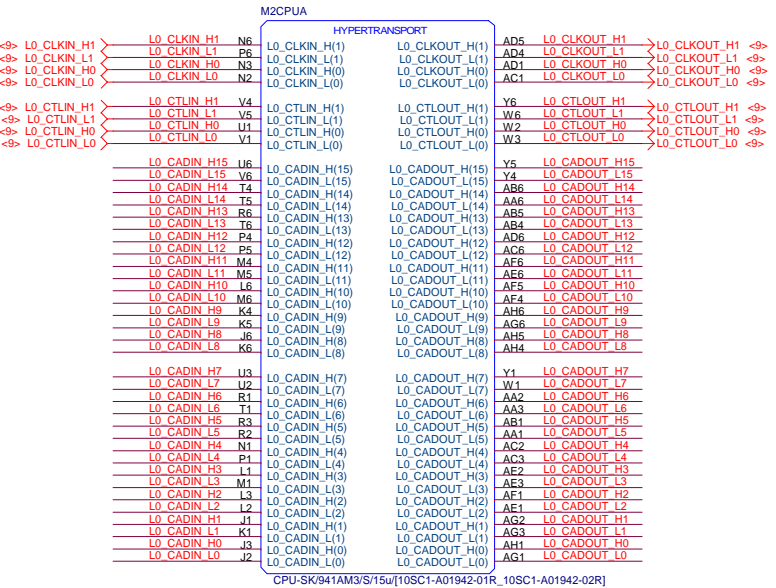
			
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COVER SHEET			
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www.xinxunwei.com 400-800-9990
RS780L CUSTOMER DESKTOP DESIGN



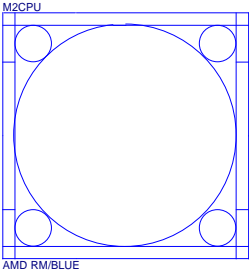
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L0_CADIN_H[0..15] <L0_CADIN_H[0..15] <9>

L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] <9>
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] <9>



CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B



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TitleCPU HYPER TRANSPORT

SizeCustom

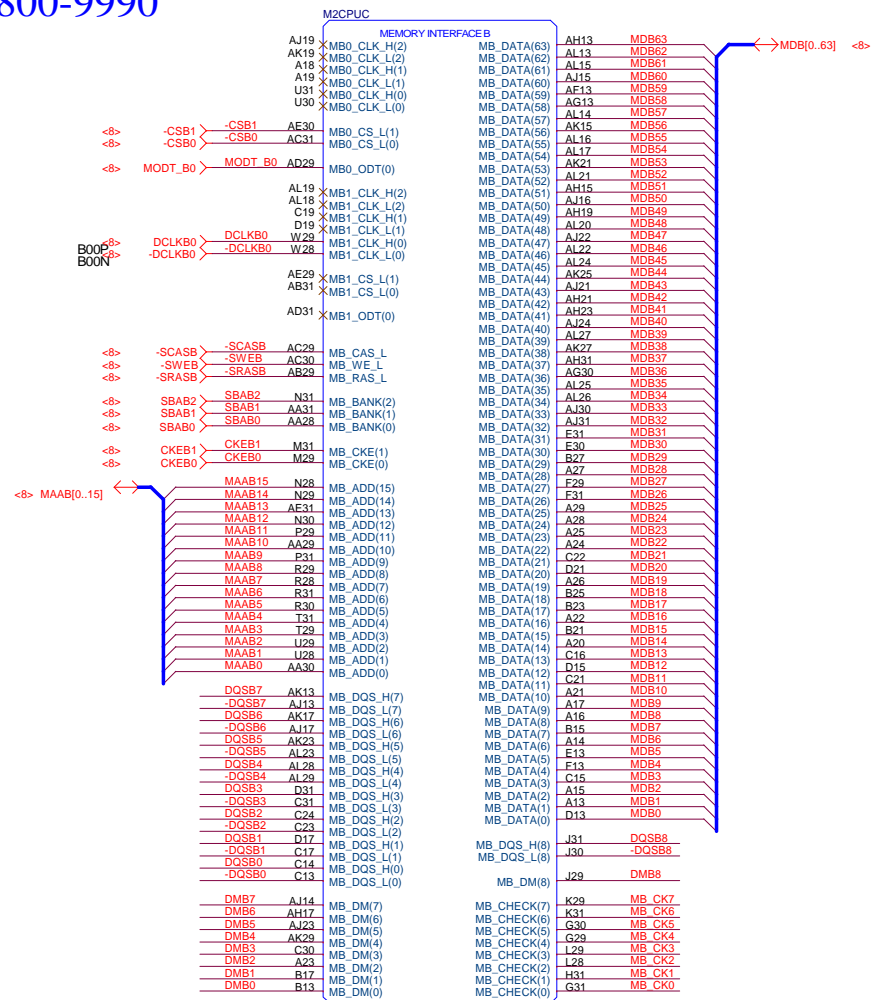
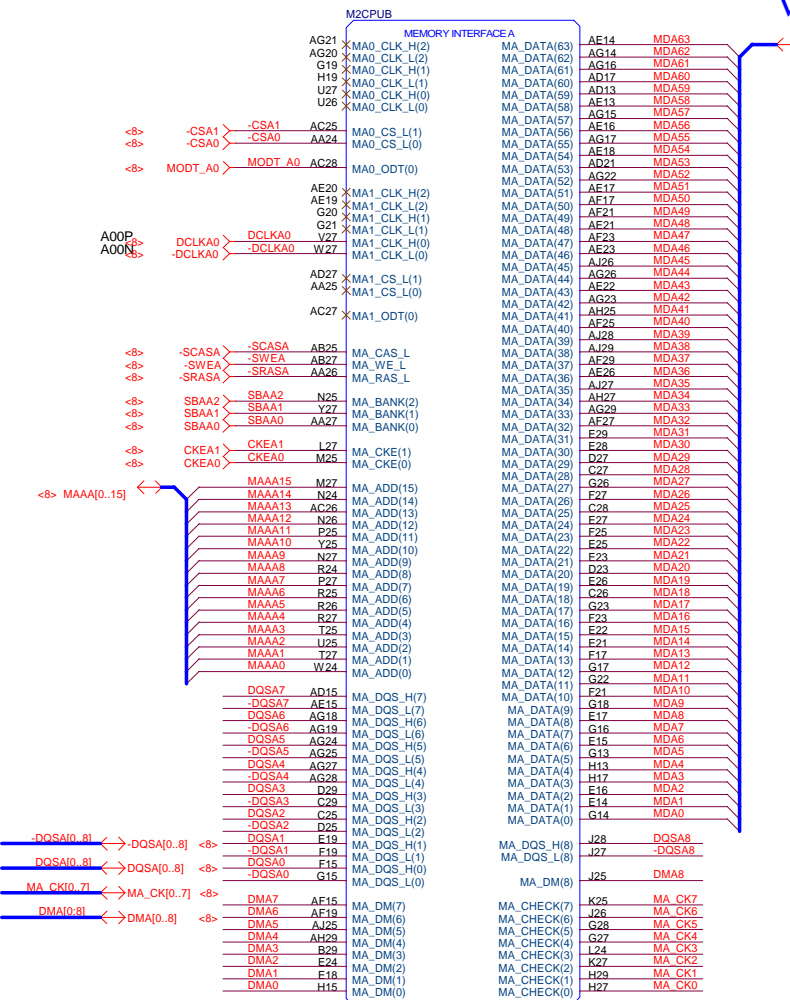
Document NumberGA-78LMT-S2P

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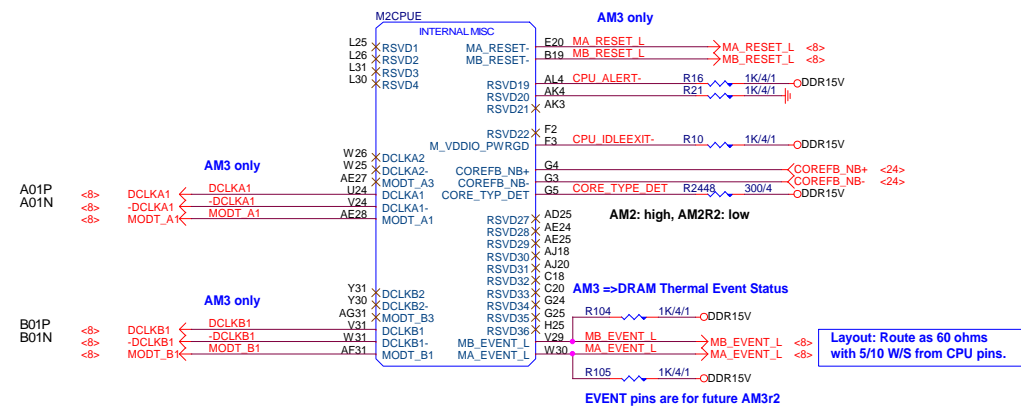
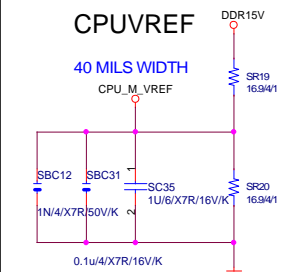
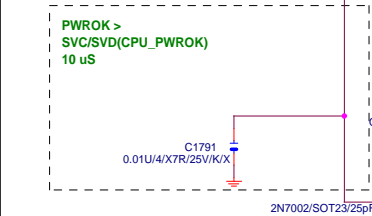
Rev5.02

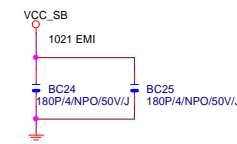
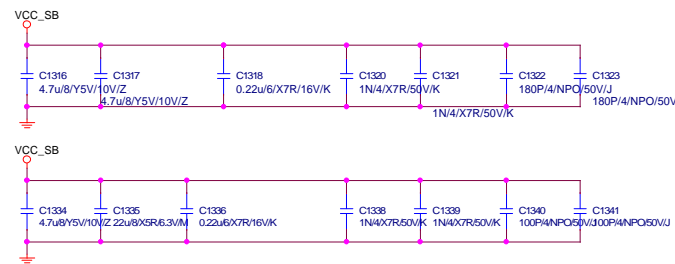
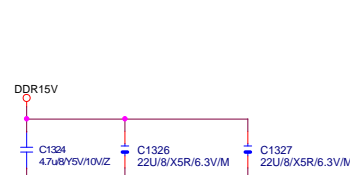
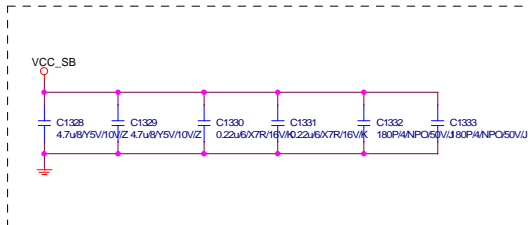
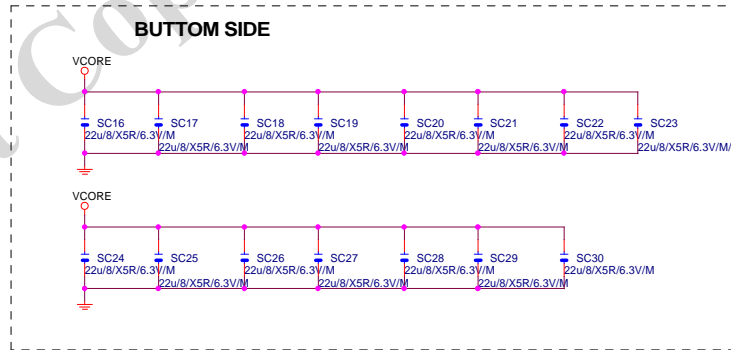
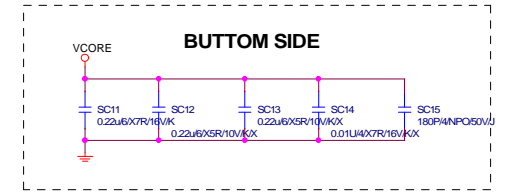
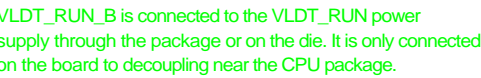
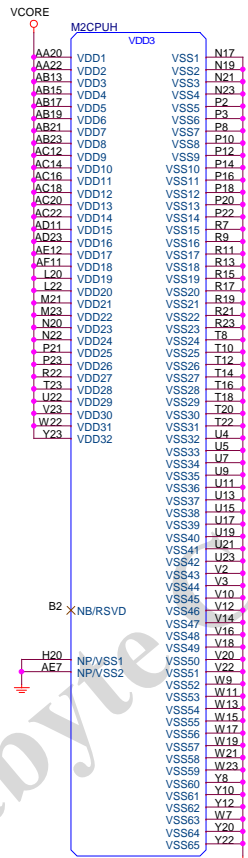


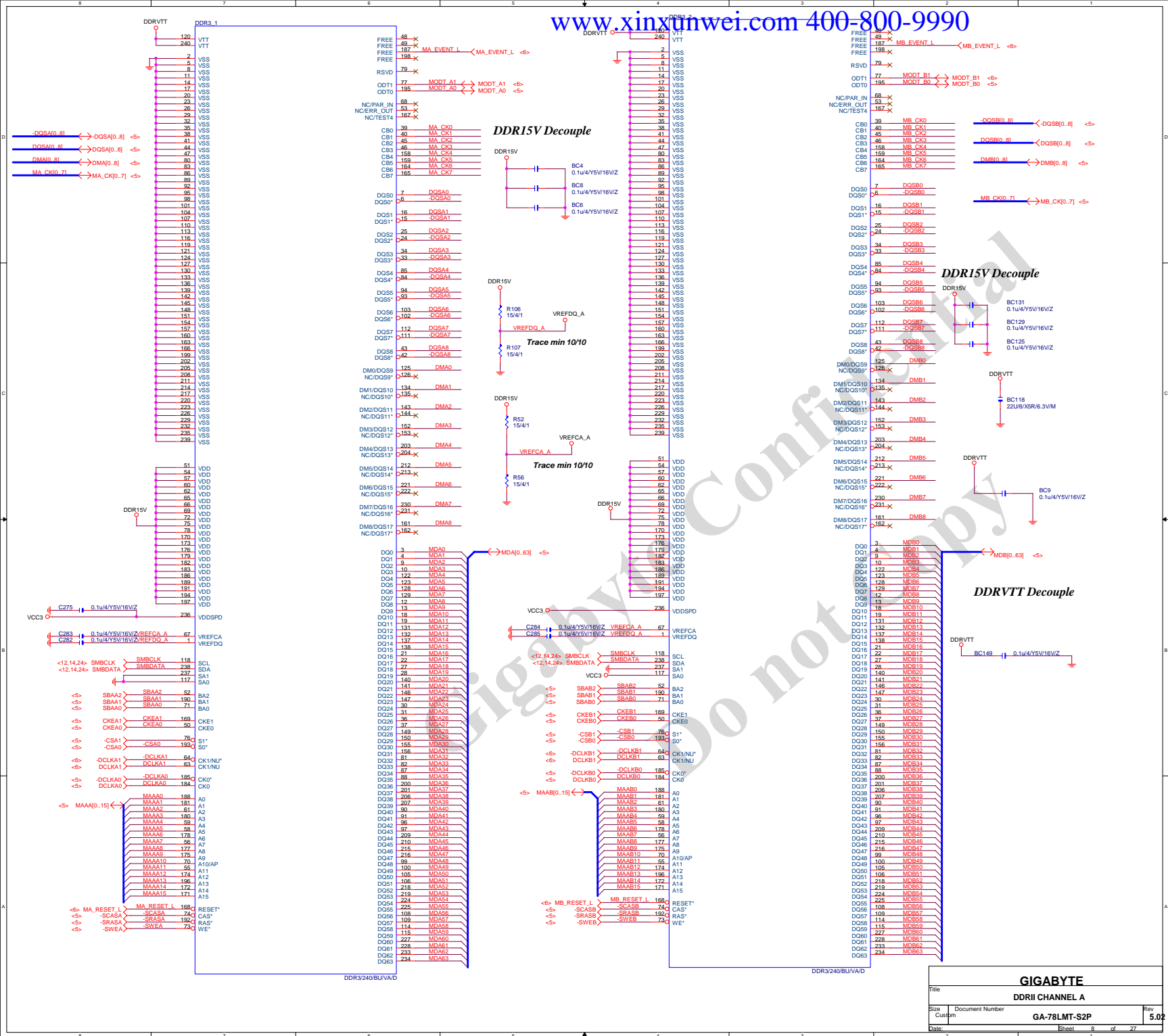
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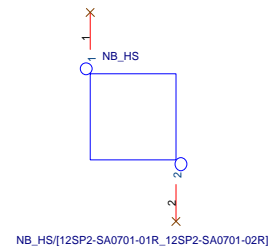
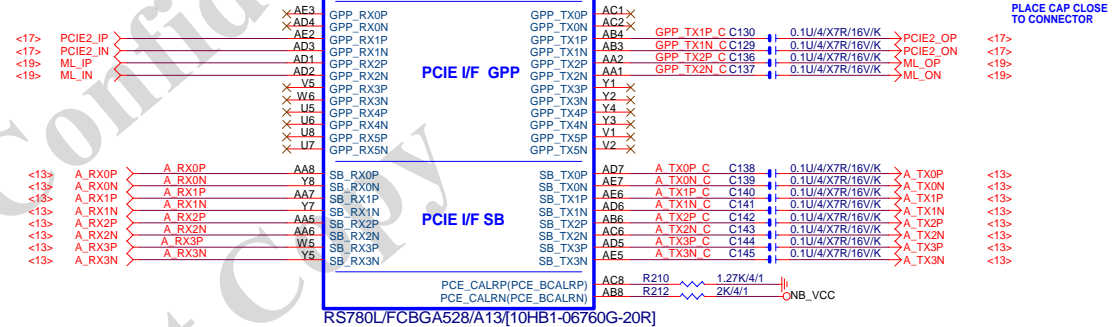
CPU DDRII MEMORY

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Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

RS740_DFT_GPIO1 R272 150/4/1

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

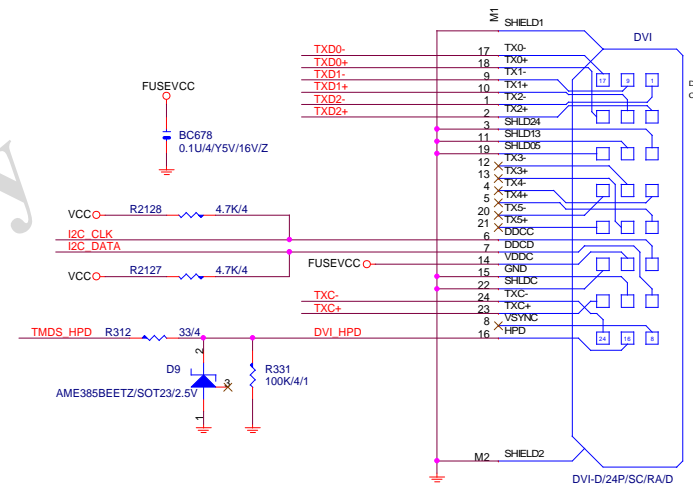
<21> DAC_VSYNC << R276 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly
R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

<21> DAC_HSYNC << R285 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)



PART 3 OF 6

CRT/TVOUT

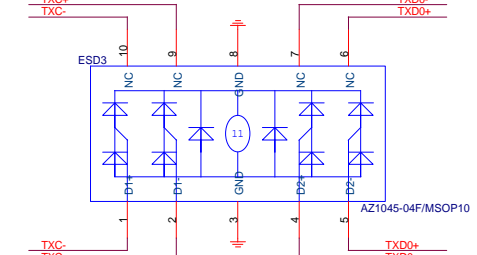
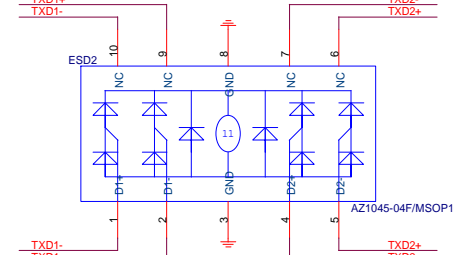
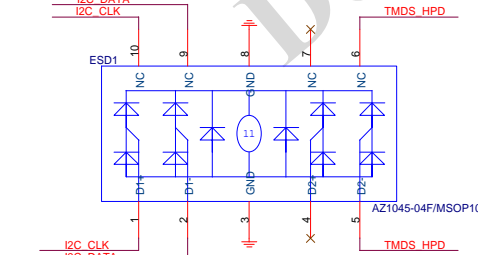
LVTM

PM PLL PWR

CLOCKS

MIS.

RS780L/FCBGA528/A13/[10HB1-06760G-20R]



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RS780 SYSTEM I/F, STRAP

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Rev 5.02

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC

GROUND

RS780L/FCBGA528/A13[10HB1-06/60G-20R]

Please use 1mm pad size,
place all ELT test pads
on bottom side only

PART 5/6

POWER

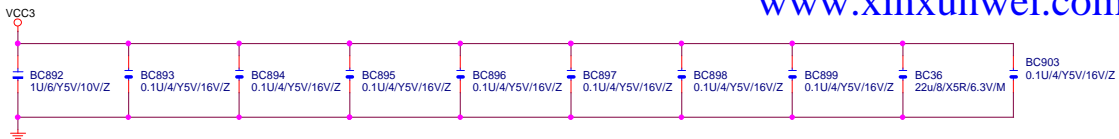
POWER

RS780L/FCBGA528/A13[10HB1-06/60G-20R]

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Title
RS780 POWER & GNDSize
Custom
Document Number
GA-78LMT-S2PRev
5.02

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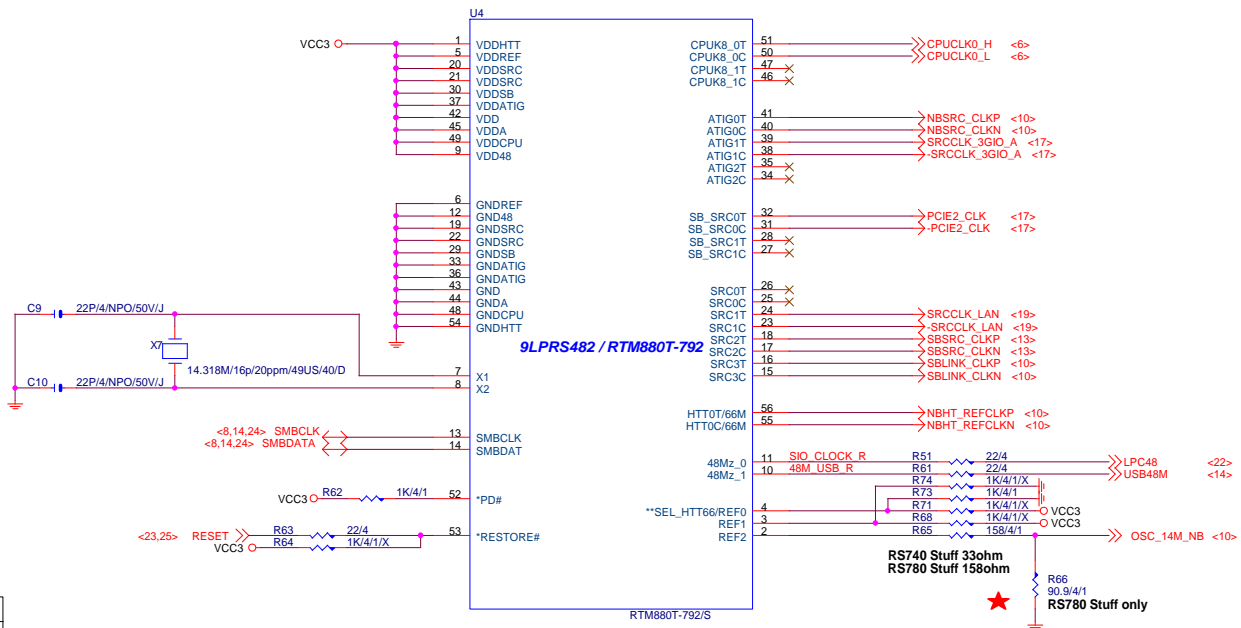


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLCKS INPUT TABLE

NB CLCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0			OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)	
	High	66MHz 3.3V single ended HT clock.	

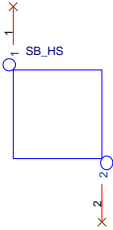
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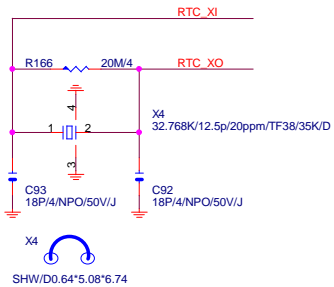


PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO U600

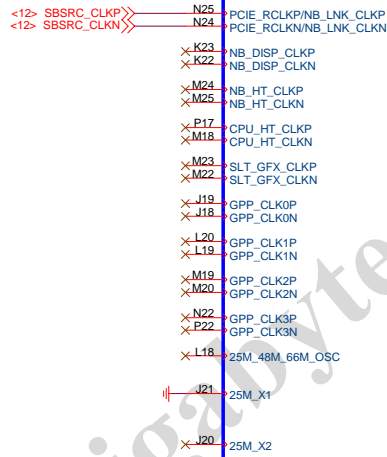
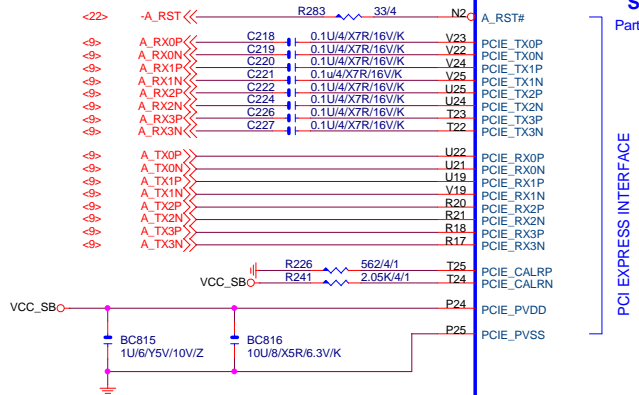
S.B HEATSINK



SB_HS[12SP2-030005-42R_12SP2-030005-43R]



X4
SHW/D0.64*5.08*6.74



Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

SB700

Part 1 of 5

PCI EXPRESS INTERFACE

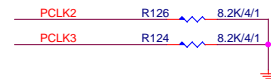
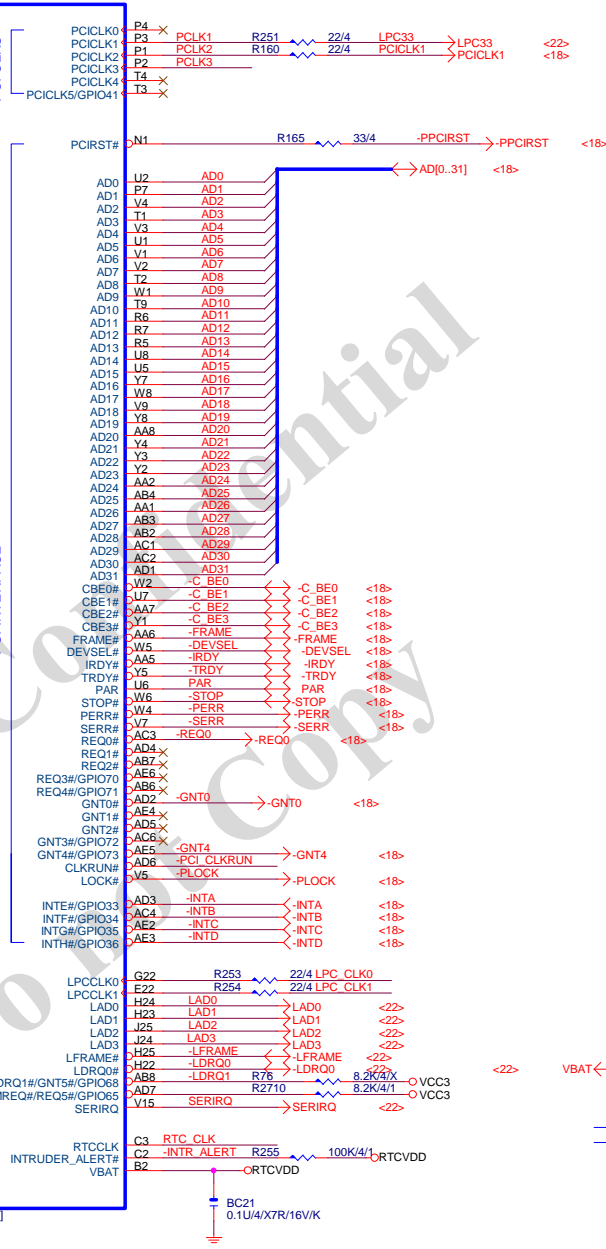
PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC



PULL HIGH
PULL LOW

PCLK2
WATCHDOG TIMER
ON NB_PWRGD
ENABLED
WATCHDOG TIMER
ON NB_PWRGD
DISABLED
DEFAULT

PCLK3
USE
DEBUG
STRAPS
IGNORE
DEBUG
STRAPS
DEFAULT

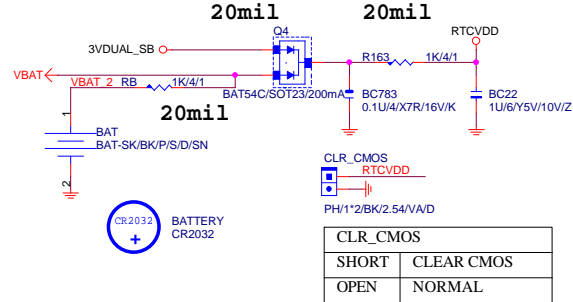


LPC_CLK0
LPC_CLK1

PULL HIGH
PULL LOW

IMC
ENABLED
AOD Extreme
DISABLED
DEFAULT

CLKGEN
ENABLED
CLKGEN
DISABLED
DEFAULT

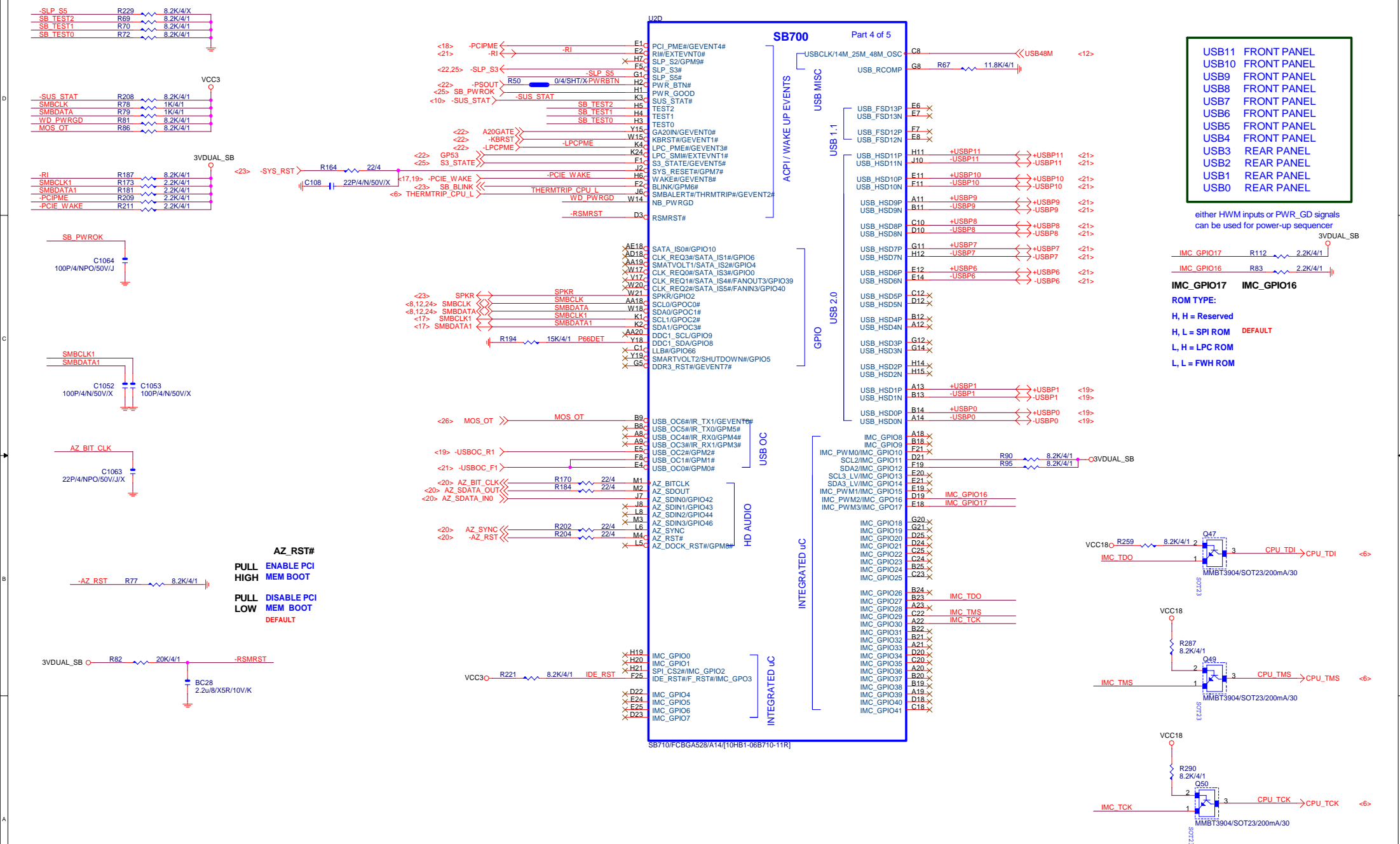


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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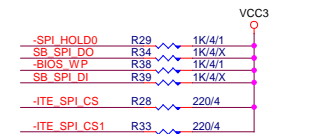
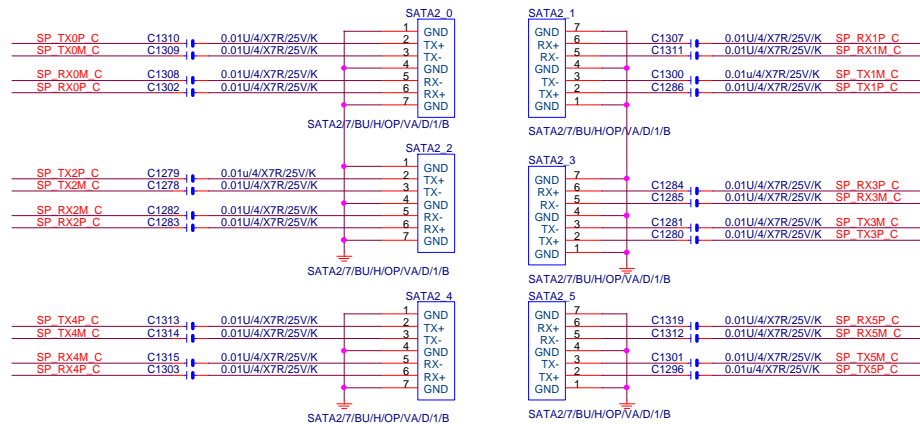
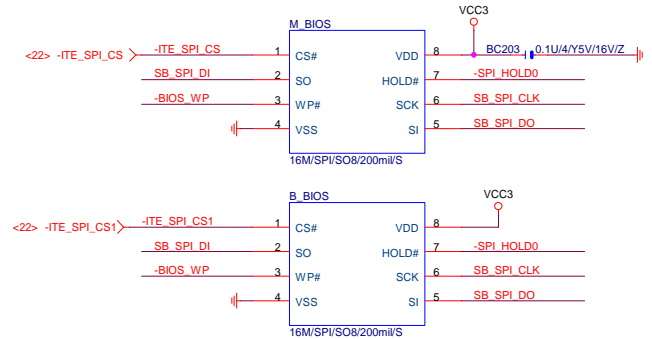
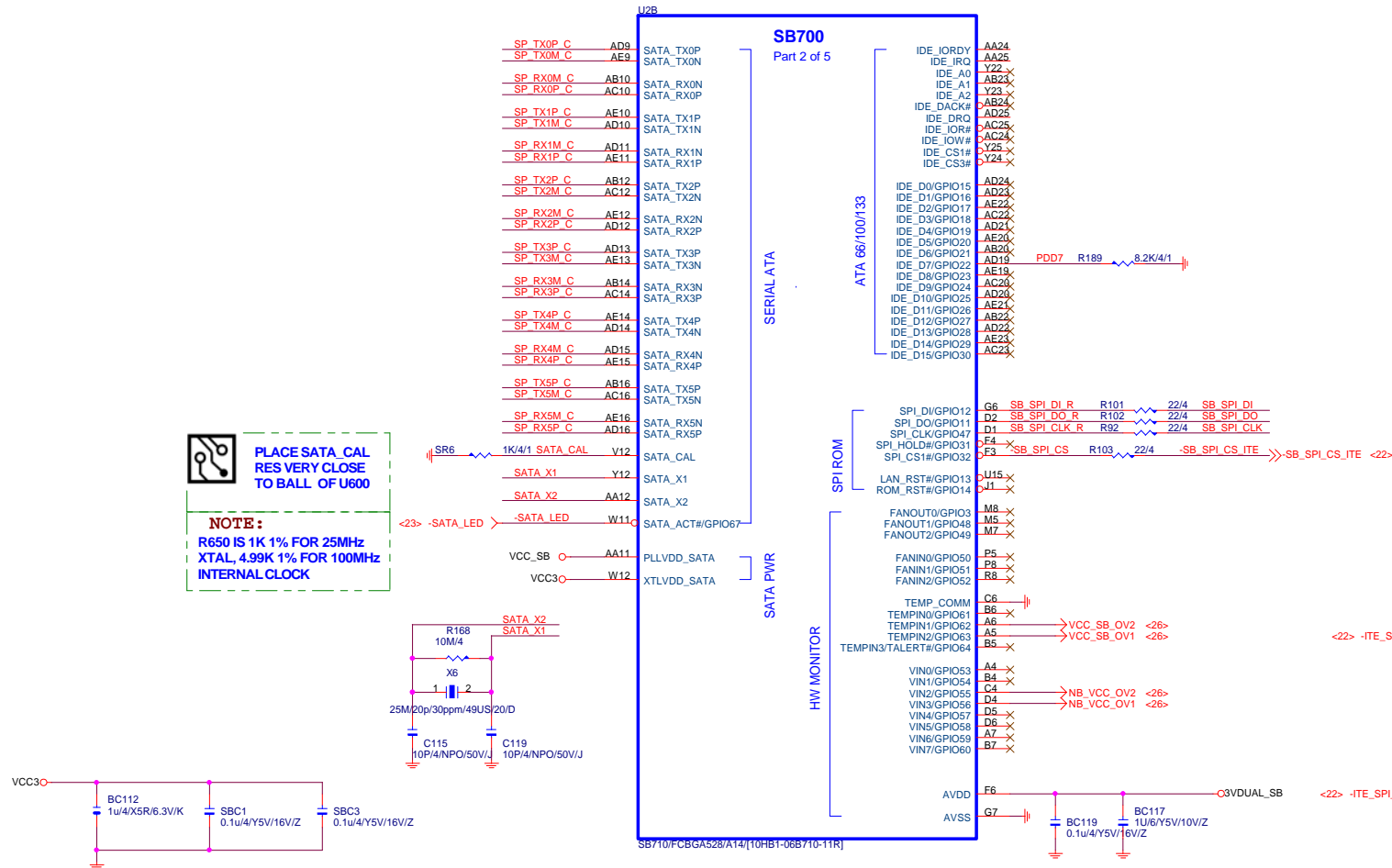
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Size Custom	Document Number GA-78LMT-S2P	Rev 5.02
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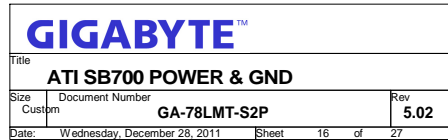


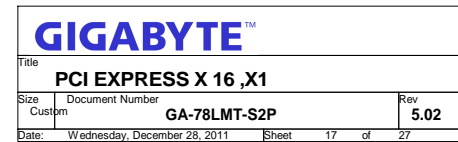
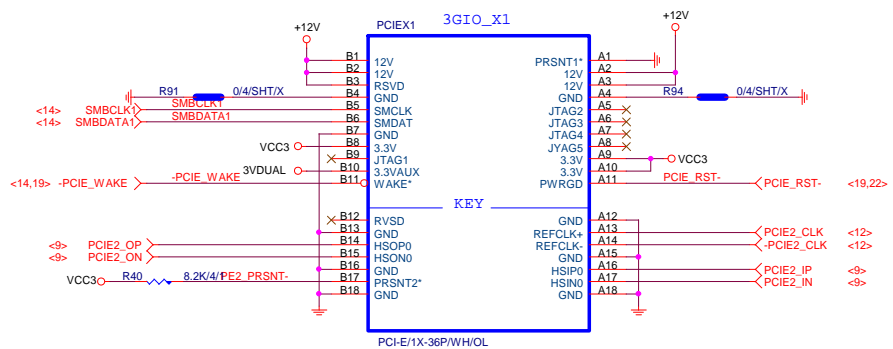


PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

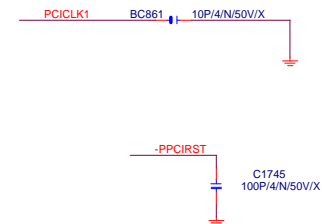
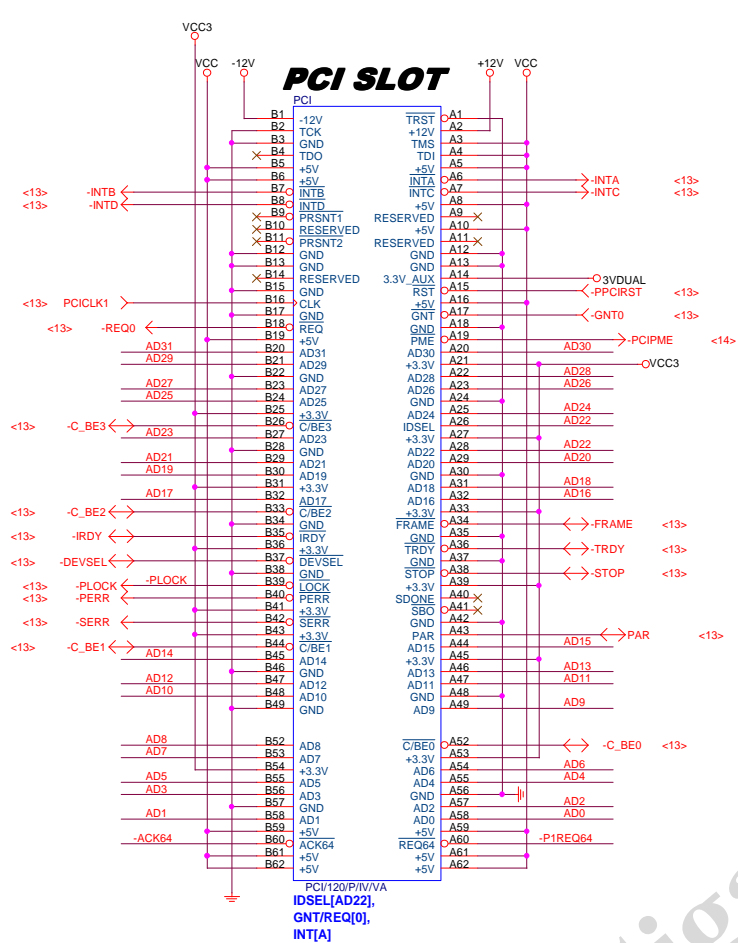




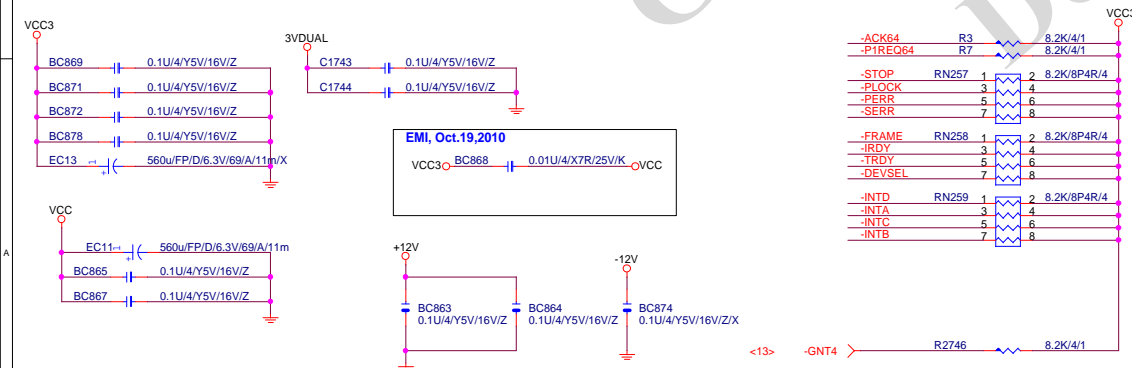


PCI SLOT 1,2

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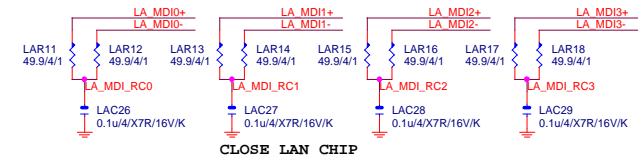


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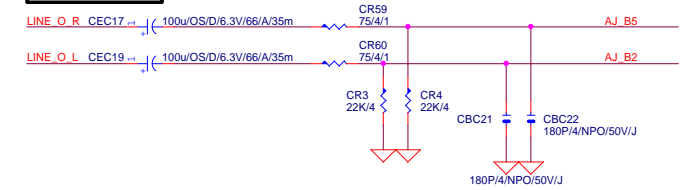


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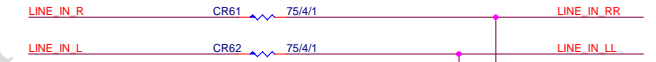
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Size	Document Number	GA-78LMT-S2P		Rev
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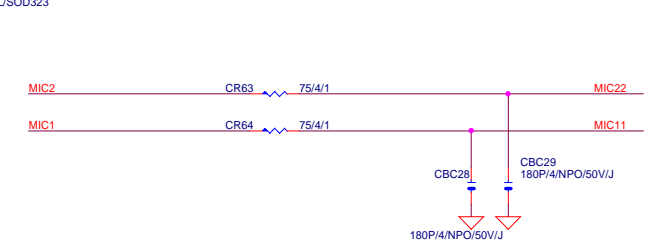
LINE OUT FRONT OUT



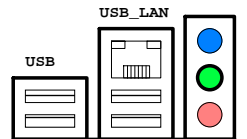
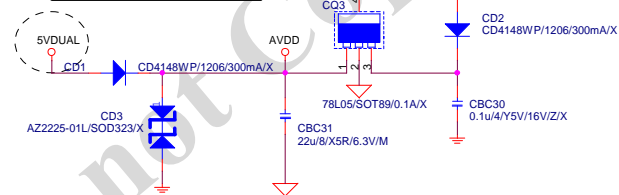
LINE-IN



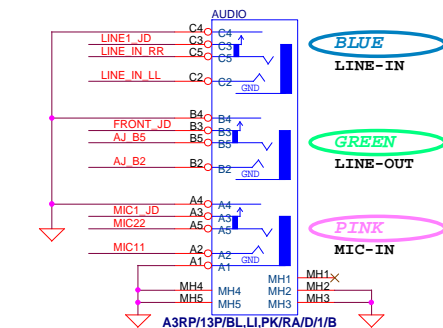
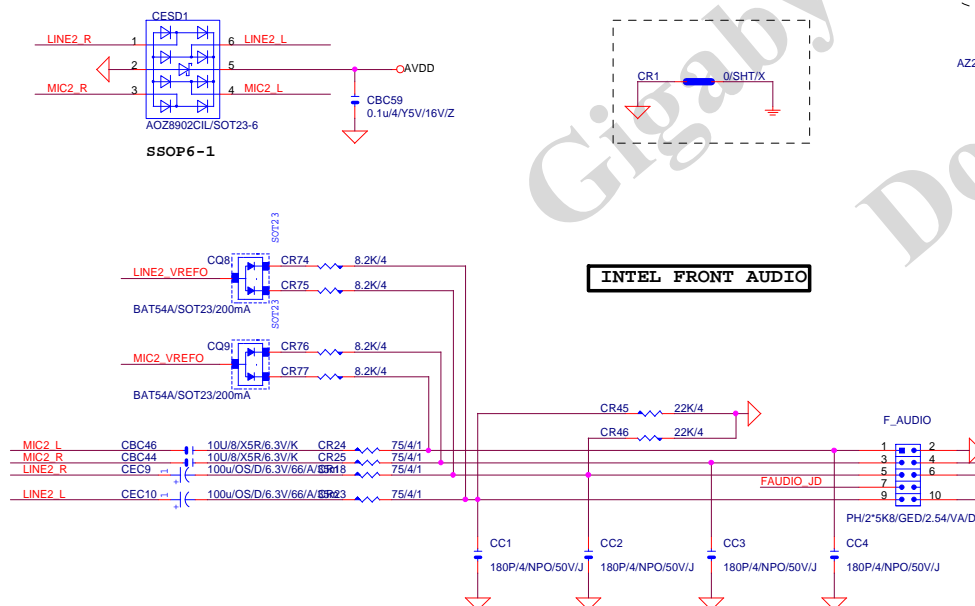
MIC



CODEC POWER/EMI PAD

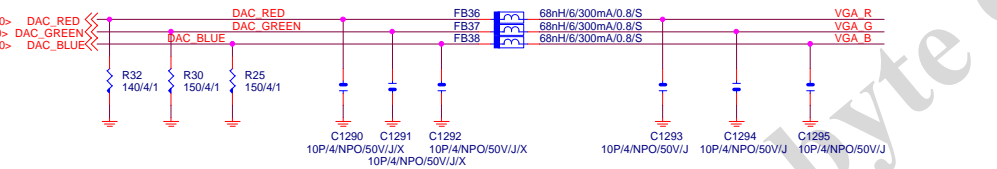
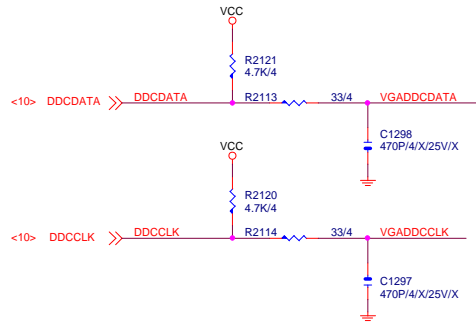
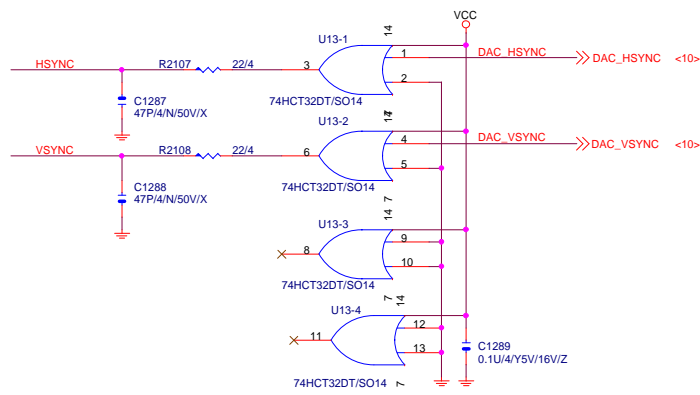


INTEL FRONT AUDIO

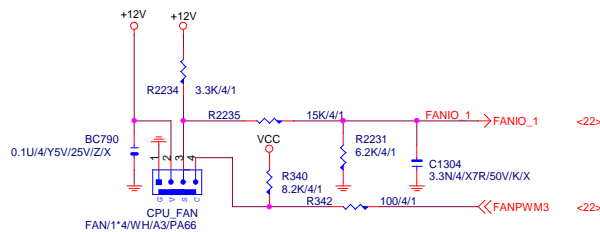


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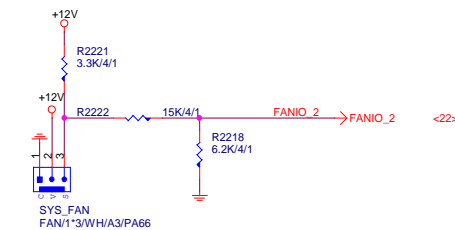
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ALC887-VD2			
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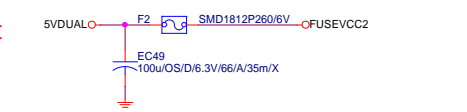
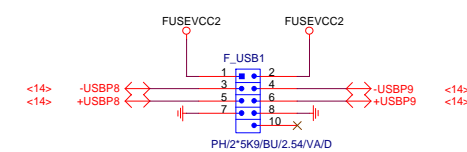
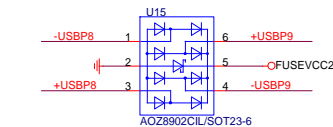
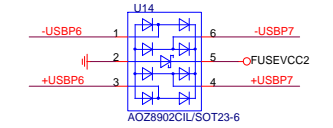
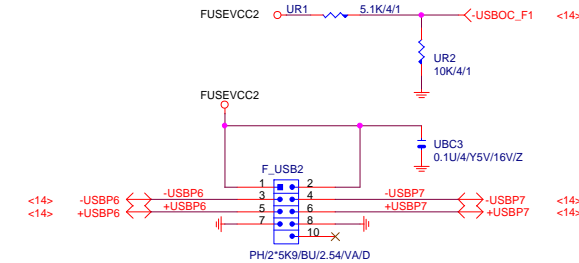
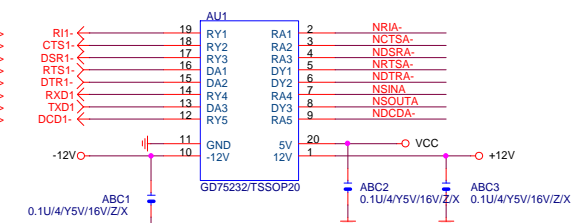
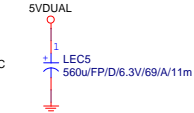
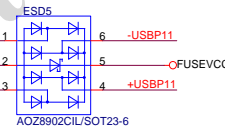
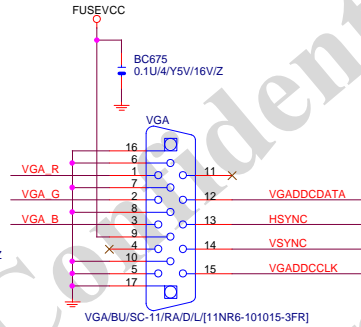
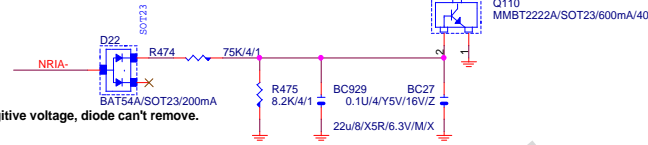
CPU_FAN

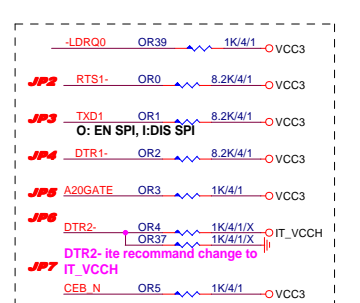
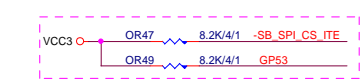
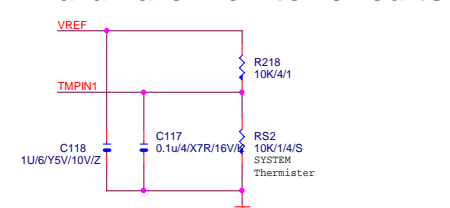
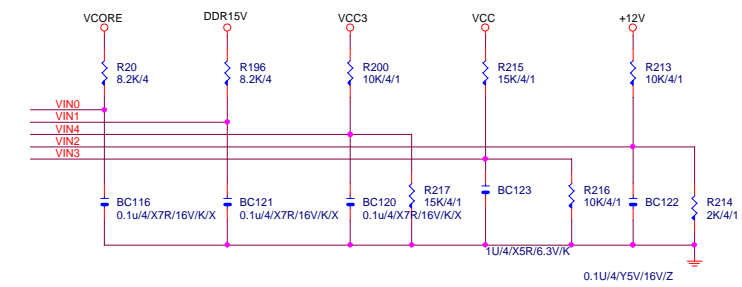
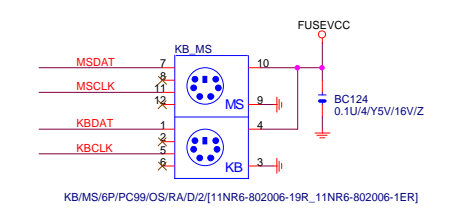
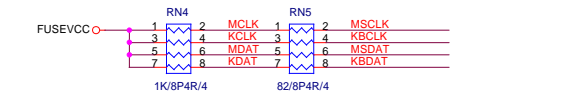
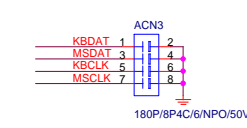
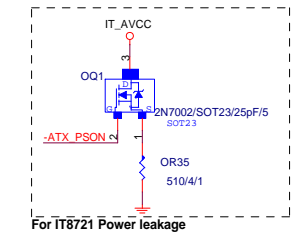


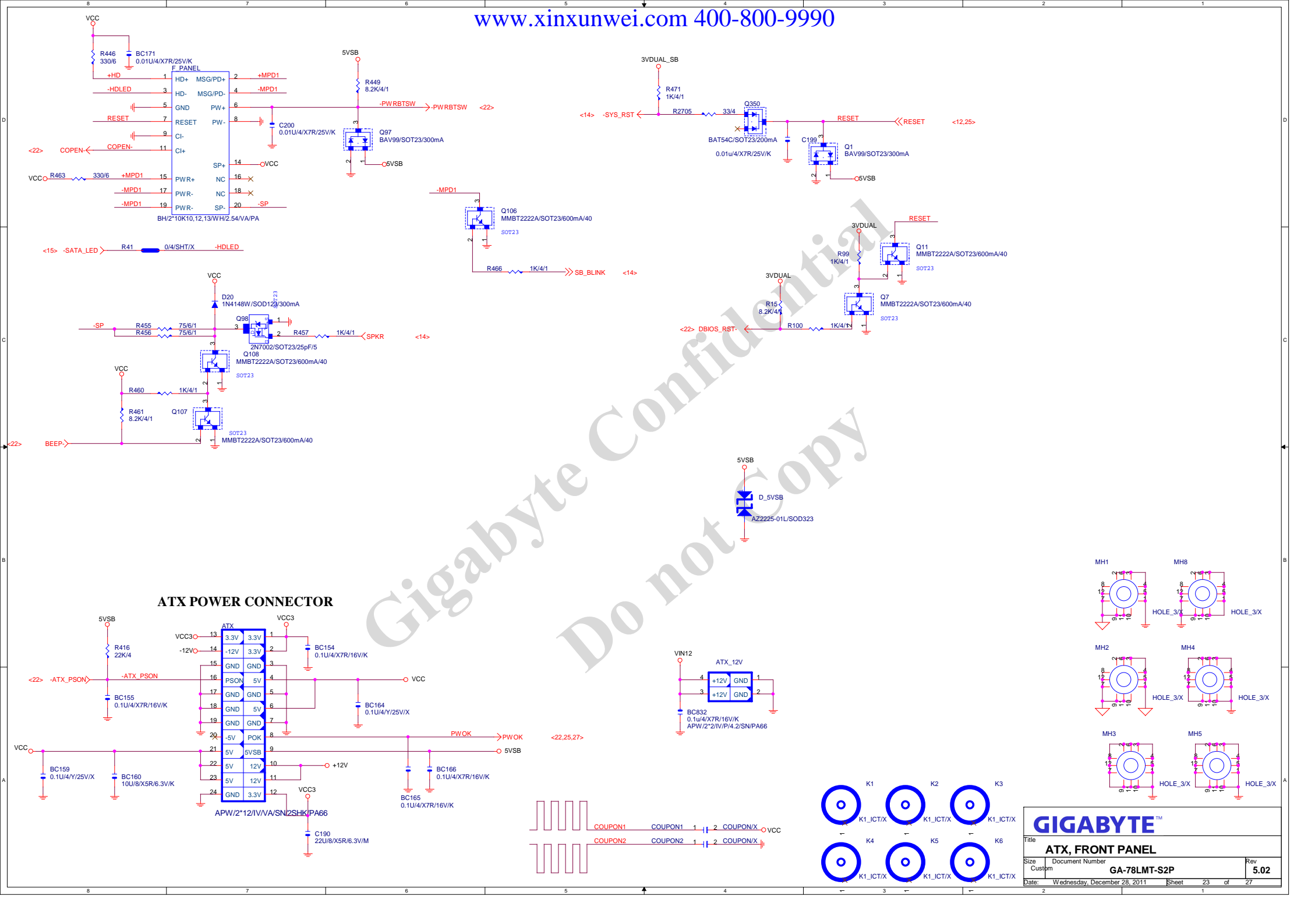
SYSTEM FAN



Negative voltage, diode can't remove.



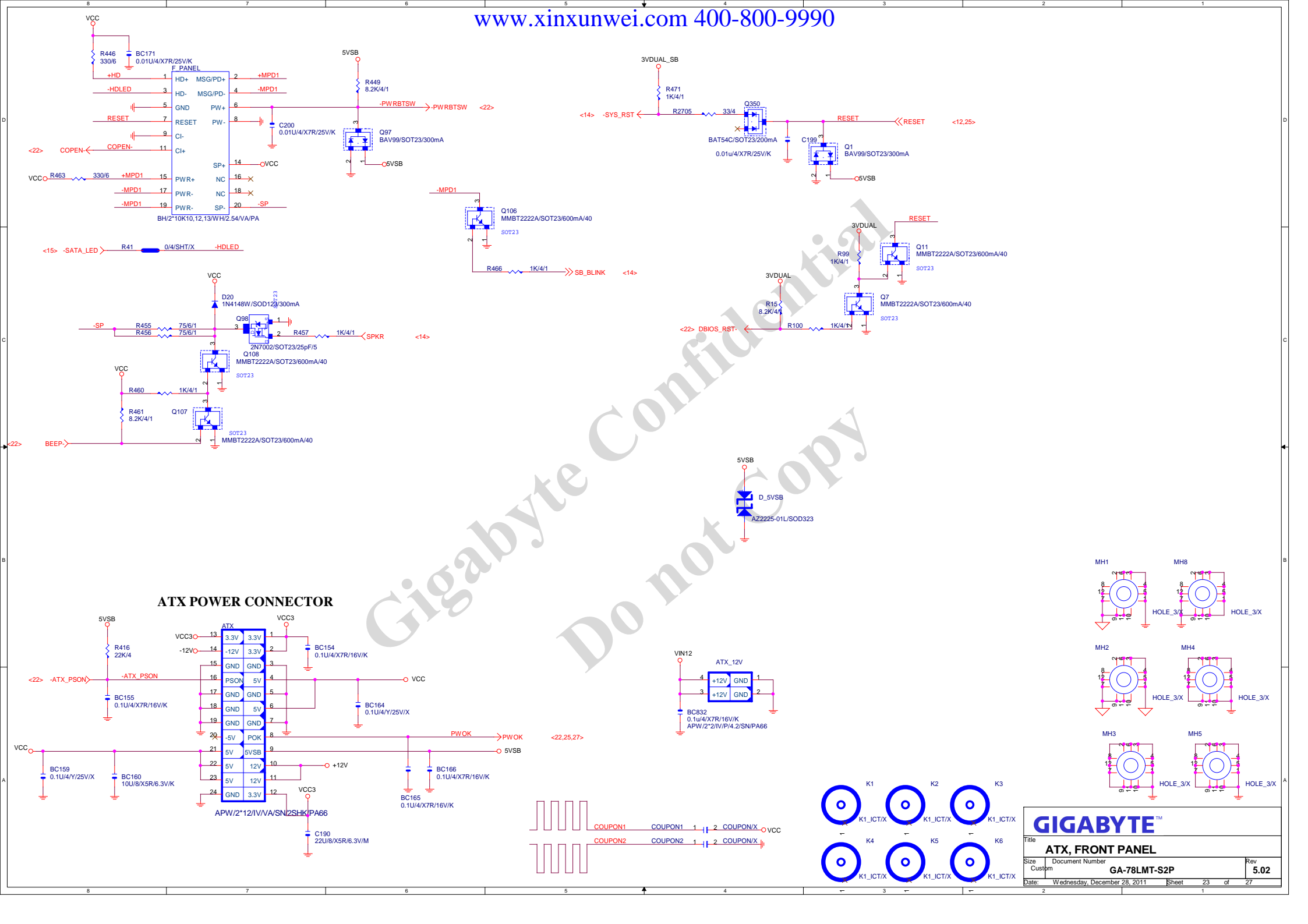
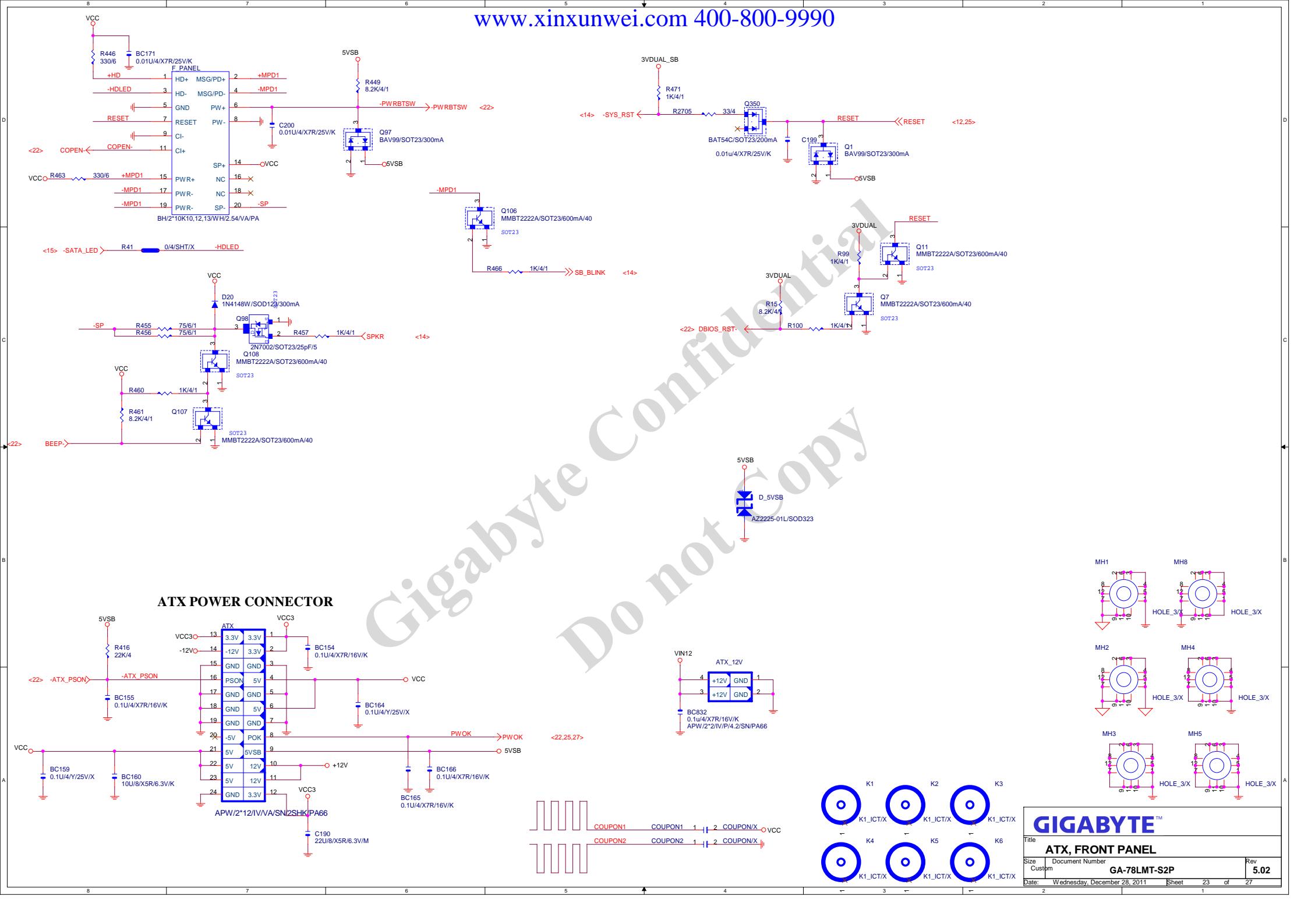
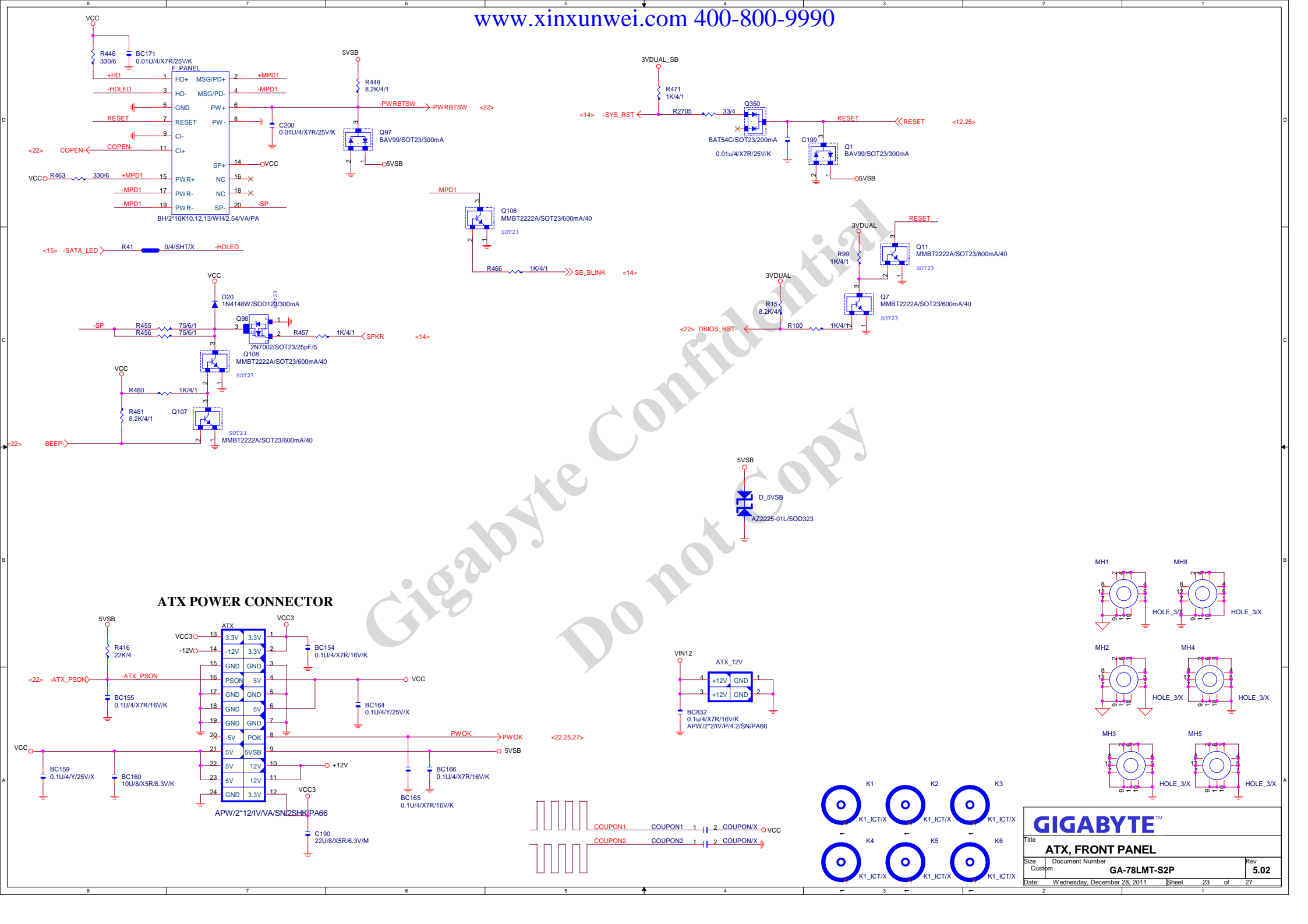
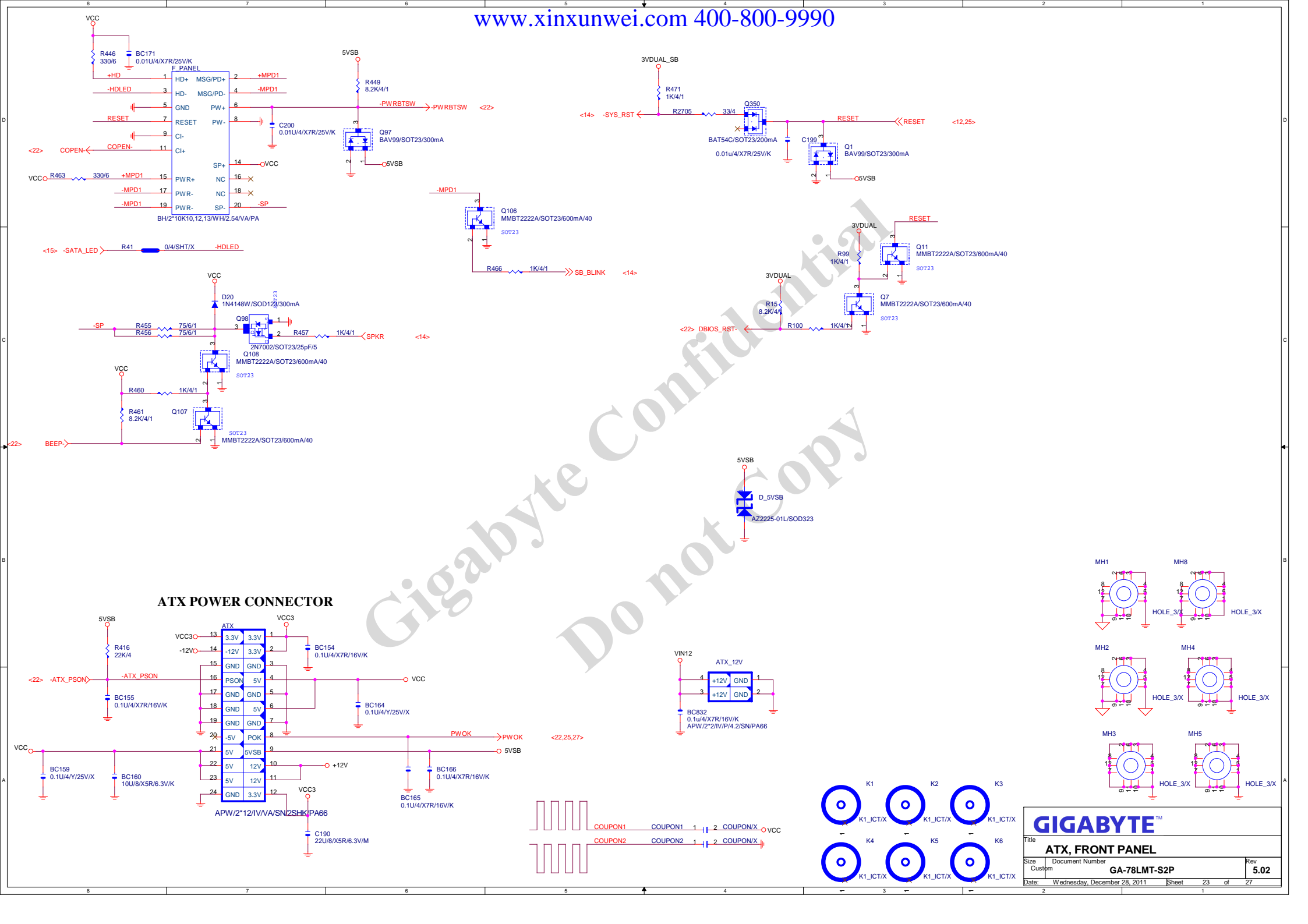


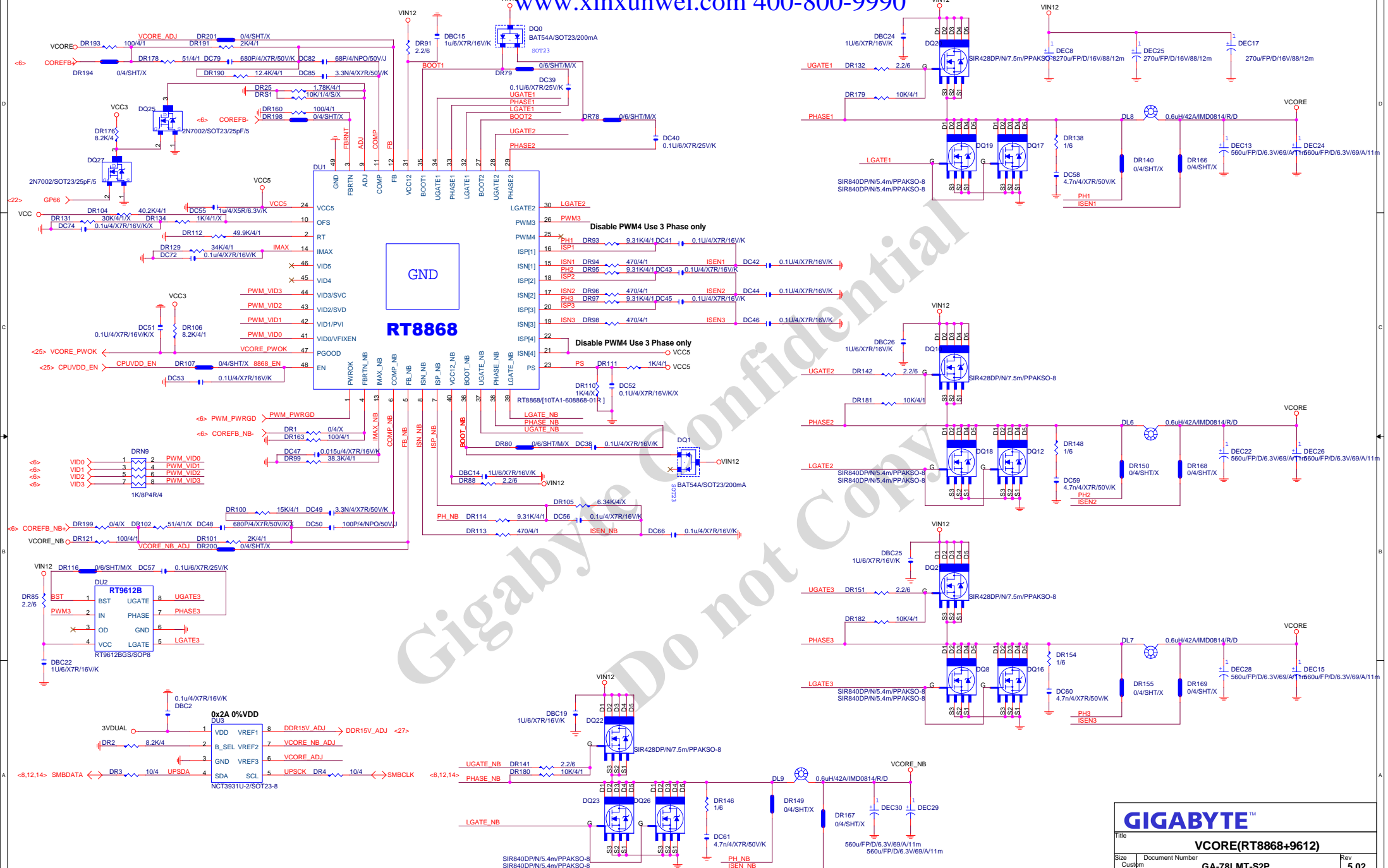


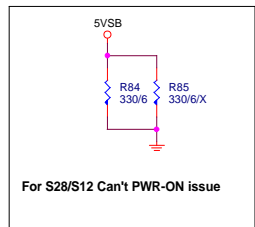
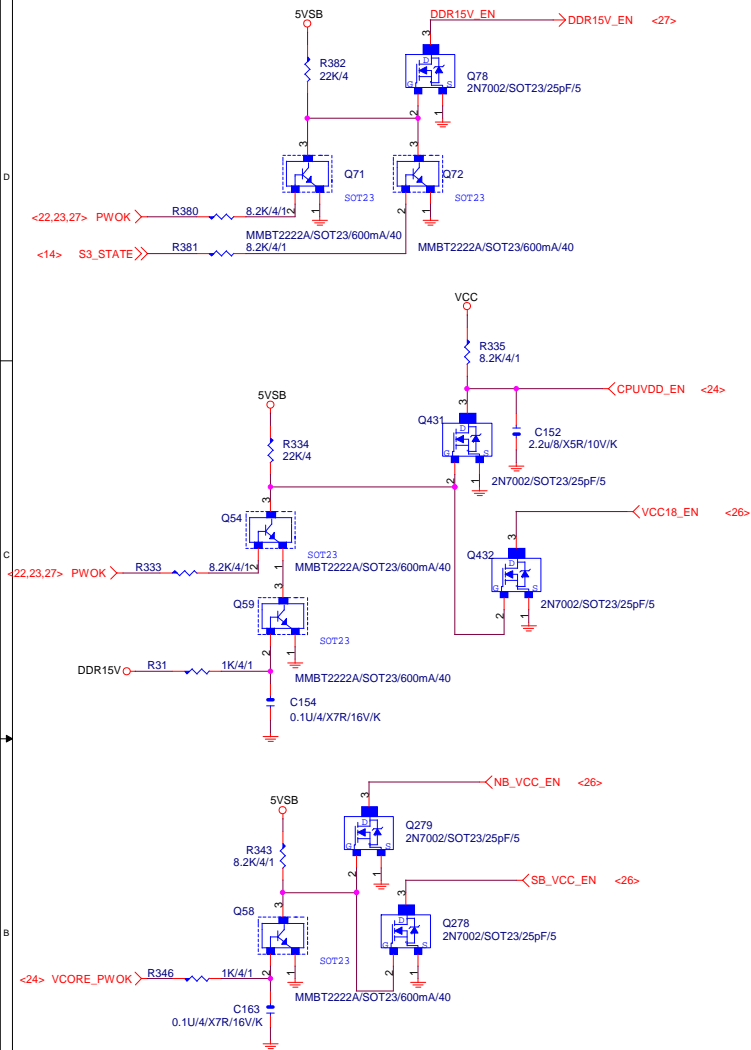
www.xinxunwei.com 400-800-9990

ATX POWER CONNECTOR

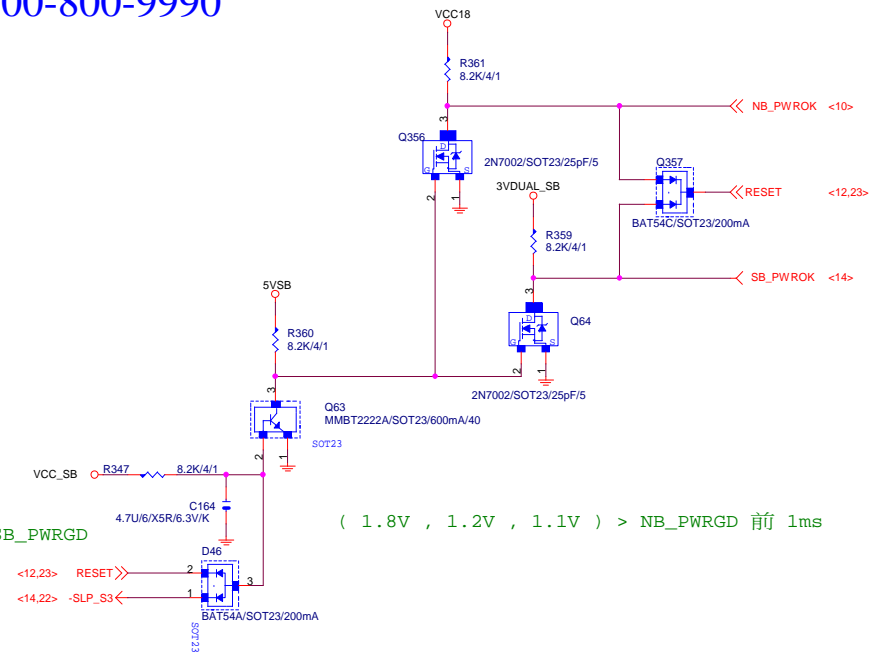
GIGABYTE
Title: ATX, FRONT PANEL
Size: Custom
Date: Wednesday, December 28, 2011
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[illegible]

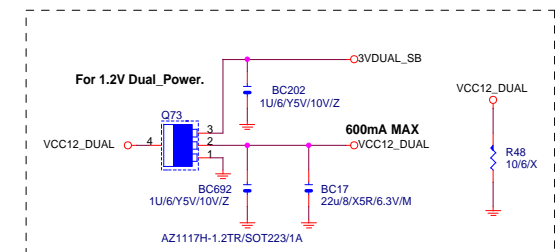
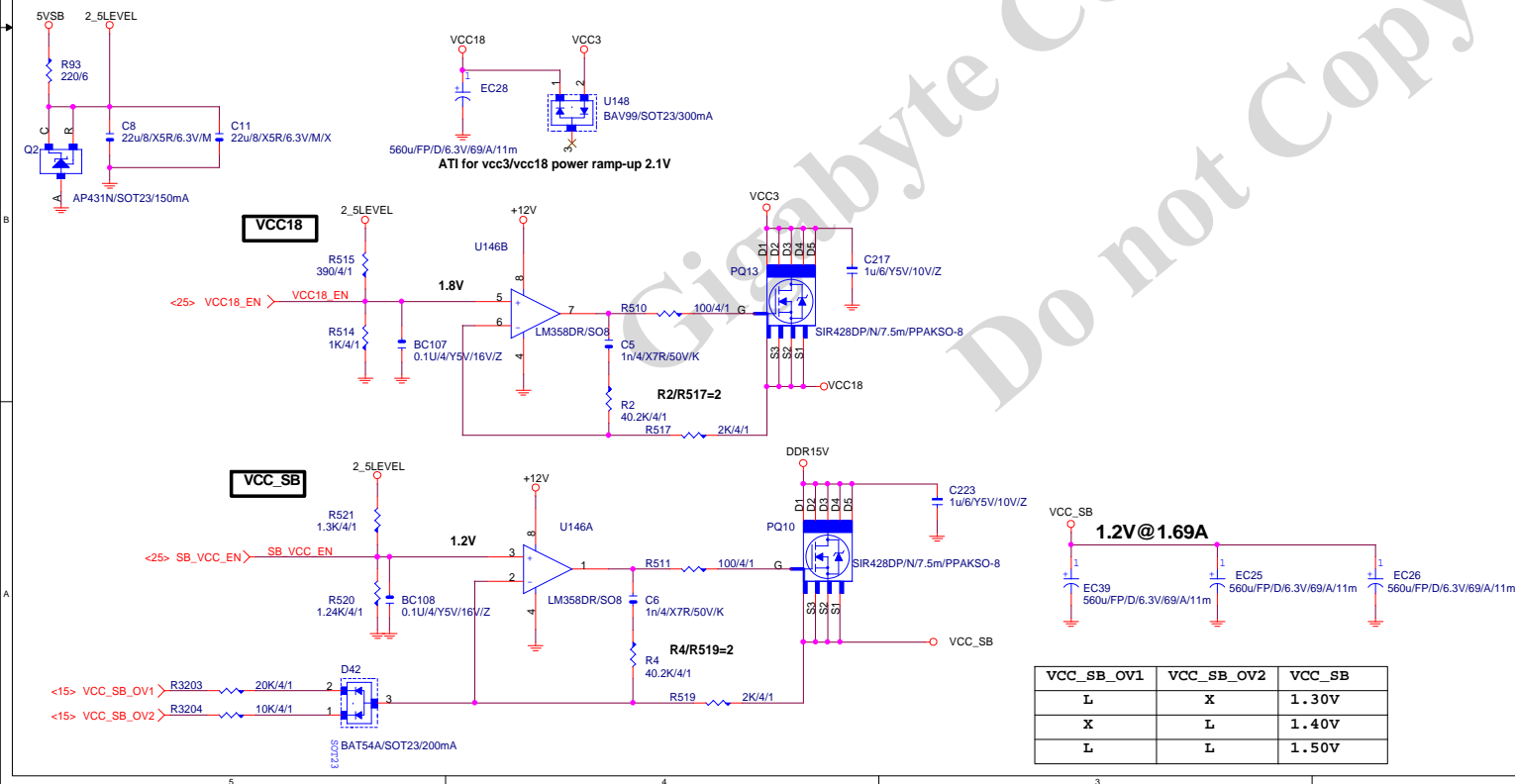
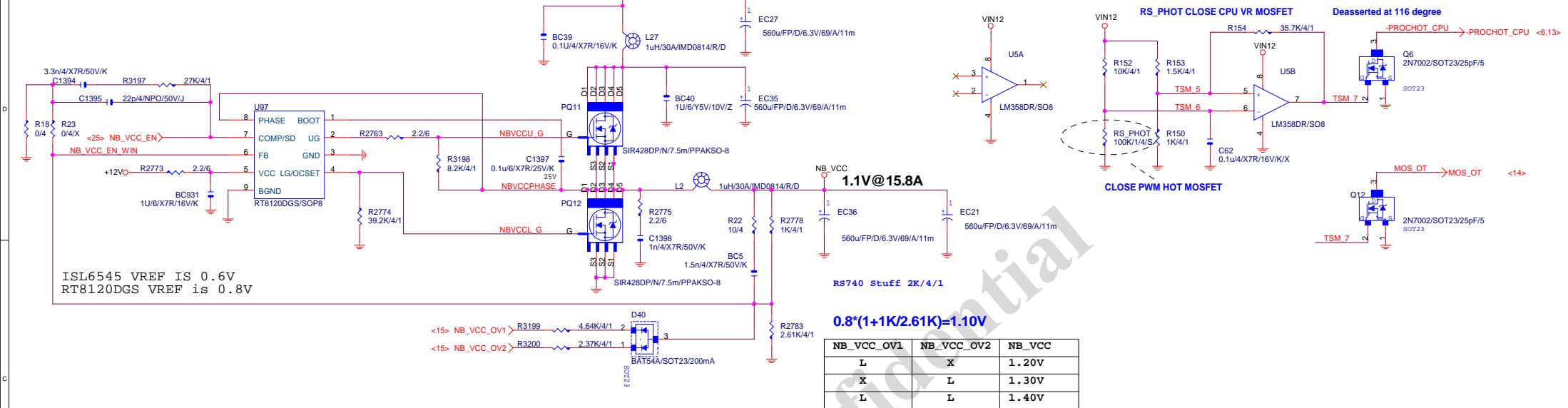




PWOK > NB_PWRGD / SB_PWRGD



(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms



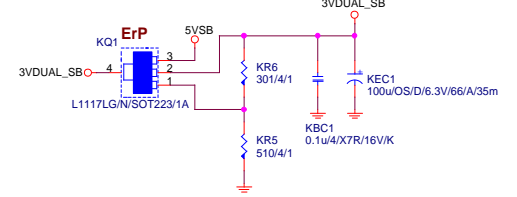
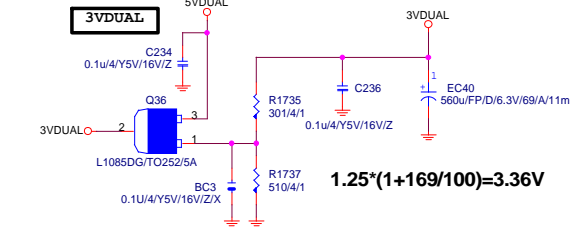
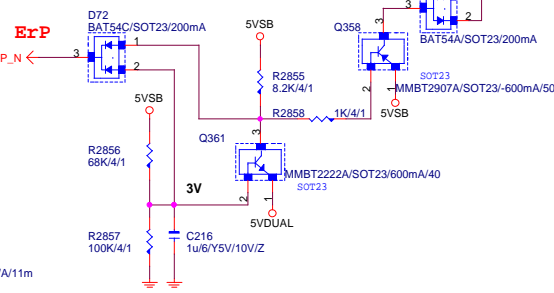
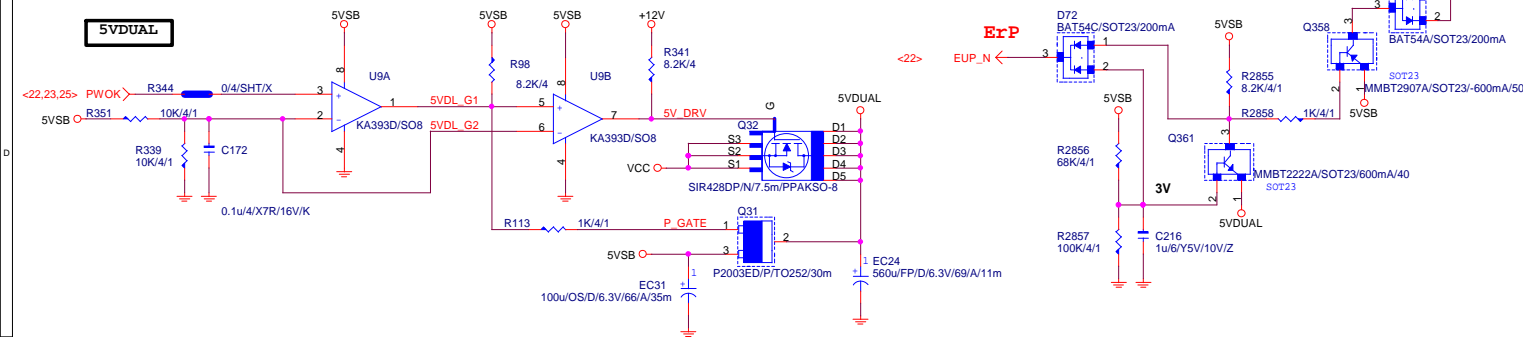
GIGABYTE™

Title NB/SB POWER,VCC12HT,VDDA25,

Size Custom GA-78LMT-S2P

Rev 5.02

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ISL6545 R9=>0, R8=>NC
RT8120 R9=>NC, R8=>0

